REMARKS

This amendment is presented in response to the Office Action dated **November 3rd, 2003** (hereafter, the Action). With this response lines 14-15 on page 8 of the specification have been canceled. Lines 1-8 on page 13 of the abstract of the disclosure have been amended. Claims 1-6 and 12-38 remain in the application. In addition to the foregoing, Applicants have amended clam 13, as above. It should be noted that the amendment to claim 13 was not made for purposes of patentability, but to simply remove lingering informalities identified therein. Applicants respectfully request reconsideration of the above referenced application as amended.

Applicants would like to thank Examiner for recognizing allowable subject matter in claims 1-6 and 23-31. As explained in more detail below, objections and rejections pointed to in the Action have been addressed.

Preliminary Issues:

In the Action, claims 12-22 are rejected under 35 USC 112, first paragraph as being unpatentable for lack of enablement in the specification. Claims 12-22 include independent claims 12 and 17. However, Examiner cites only portions of independent claim 12 when rejecting claims 12-22. Applicants respectfully submit that elements stated by the Examiner as "the equivalent representation is such that no taps are within n spaces from the input" are not included in independent claim 17. To the extent that the Examiner intended to reject claims 17-22 as lacking enablement in the specification, further clarification is requested in order to afford the Applicants their statutory right to respond in kind. Applicants respectfully assert that until such clarification is made, the next Action cannot be made final.

Objection to Disclosure:

In paragraph 1 of the Action, the Examiner objected to the disclosure because, "the "APPENDIX I" contains drawings and different lay out..." Examiner's stated position is that "A substitute specification excluding claims is required pursuant to 37 CFR 1.125(a)."

Without accepting or adopting the grounds for the request, in an effort to conclude prosecution of this matter, Applicants have amended the Specification and canceled lines 14-15 of page 8, which reference Appendix I without prejudice. In addition, Appendix I has been removed from the application. Accordingly, Applicants respectfully request that this objection to the Specification be withdrawn.

Objection to the Abstract of the Disclosure:

In paragraph 2 of the Action, the Examiner objected to the abstract of the disclosure because, "legal phraseology is used in this paragraph (i.e. "comprising")." Examiner's stated position is that "Correction is required. See MPEP § 608.01(b)

Without accepting or adopting the grounds for the request, in an effort to conclude prosecution of this matter, Applicants have amended the Abstract of the Disclosure by deleting lines 1-8 and adding new language. Accordingly, Applicants respectfully request that this objection to the Abstract of the Disclosure be withdrawn.

Claim Rejections:

In paragraph 3 of the Action, claims 12-22 are rejected under 35 U.S.C. 112, first paragraph for lack of enablement in the specification; and claims 32-35 are rejected under 35

U.S.C. 103(a) as being unpatentable over either Shimada (US Patent 6,192,385) or Shimada (US Patent 5,566,099). Applicants address these rejections in turn, below.

§112, first paragraph Rejection of Claims 12-22:

In paragraph 3 of the Action, claims 12-22 are rejected under 35 U.S.C. 112, first paragraph as unpatentable for lack of enablement in the specification. The rejection of claims 12-22 on this basis is respectfully traversed.

Claim 12 states:

> "A method of implementing a pseudo-random code generator:
> converting a psuedo-random code generator specification into an equivalent representation, the psuedo-random code generator specification being such that taps used to calculate an output include at least one tap within n spaces from the input, the equivalent representation is such that no such taps are within n spaces from the input; and
> implementing the equivalent representation such that multiple new state bits are calculated at the same time."

In the Action, the stated position is that the specification "does not reasonably provide enablement for "the equivalent representation is such that no taps are within n spaces from the input"." Further, the Action provides that "applicants do show the pseudo-random code generator has "taps used to calculate an output include at least one tap within n spaces from the input", e.g. see two pair decomposed "LFSRs" of Fig. 2. The Fig. [2] merely shows the "gold code generator" (60) is separated in two portions with some modifications but they still have the "taps are within n spaces from the input". Applicants respectfully disagree.

In the Action reference is made to Fig. 2 and the showing of gold code generator (60). Applicants respectfully submit that the gold code generator (60) referred to in the Action is an example embodiment of a *psuedo-random code generator specification*. Further the gold code

generator (60) is converted into an *equivalent representation* which is illustrated by elements (62) and (64). For an example see Application, page 5, lines 11-14. Thus, element (60) is an example illustration of the elements of claim 12 of "the pseudo-random code generator specification, being such that taps used to calculate an output include at least one tap within n spaces from the input." Additionally, as will be described below, elements (62) and (64) are example illustrations of the elements of claim 12 of "the equivalent representation is such that no such taps are within n spaces from the input."

Applicants respectfully submit that the elements of "taps used to calculate an output" may be illustrated by reference to Fig. 1 of the Application. In Fig. 1, the taps used to calculate an output are illustrated as taps made at registers 4, 7 and 18 for the first linear feedback shift register (LFSR) and registers 4, 6 and 17 for the second LFSR, e.g. see Application page 2, lines 24-28. Further, Fig. 1 shows the input as register 24 for both the first and second LFSRs. As illustrated in Fig. 1, the taps *used to calculate an output* are 24 minus 18 or *6 spaces from the input* for the first LFSR and 24 minus 17 or *7 spaces from the input* for the second LFSR. Thus, Fig. 1 shows that *"n"* as stated in claim 12 *equates to 6* for the first LFSR *and 7* for the second LFSR.

Applicants further respectfully submit that the equivalent representation illustrated in (62) and (64) illustrates that the *only tap used to calculate an output* is at register 0. Further, the other taps at registers 0 and 3 for LFSRA and registers 0-3 of LFSRB in (62) are feedback taps and are *not taps used to calculate an output*. Consequently, Fig. 2 illustrates that the taps at register 0 that are used to calculate an output in (62) and (64) are 24 spaces from the input at register 24. Thus, since 24 spaces is greater than the 6 or 7 spaces for "n" as stated above for (60), *no taps used to calculate an output are within 6 or 7 spaces from the input* for the equivalent

representations illustrated in (62) and (64). Therefore, Figures 1 and 2 do enable any person skilled in the art to which the invention in claim 12 pertains.

Thus, in summary, Applicants respectfully submit that the specification and Figures 1 and 2 meet the requirements stated in 35 U.S.C. 112, first paragraph and enable any person skilled in the art to which the invention in claim 12 pertains. Therefore, for at least the foregoing reasons, it is respectfully requested that the Examiner withdraw rejection of claims 12-22.

§103(a) Rejection of Claims 32-35:

In paragraph 4 of the Action, claims 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Shimada '385 or Shimada '099. The rejection of such claims on this basis is respectfully traversed.

Claim 32 states:

> "A gold code generator comprising:
> multiple pairs of linear feedback shift registers to simultaneously produce more than one state bit and more than one output bit for each pair of linear feedback shift registers."

In the Action, the stated position is that "Shimada disclose (e.g., see Shimada '385 Figs. 5 & 8-9 or Shimada '099 Figs. 2 & 4) pseudo-random number generators having n [parallel] linear feedback shift registers (LFSRs) to simultaneously output the desired outputs." Applicants respectfully disagree.

As is well-established, to make a prima facie rejection of obviousness under 35 USC 103(a), the prior art reference (or references when combined) must disclose or suggest all the claim limitations. See MPEP 2143. In this case, as developed more fully below, Applicants respectfully submit that this burden has not been met.

Applicants respectfully disagree that either Shimada '385 or Shimada '099 disclose or suggest all the elements of e.g. claim 32. In particular, Applicants respectfully disagree that Shimada '385 Figs. 5 & 8-9 and Shimada '099 Figs. 2 & 4 disclosure of pseudo-random number generators having n [parallel] linear feedback shift registers makes claim 32 obvious to a person having ordinary skill in the art.

As presented above, claim 32 includes the feature of *multiple pairs* of linear feedback shift registers (LFSRs). In contrast to the multiple pairs of LFSRs, Shimada '385 in column 1, lines 54-57 explicitly discloses that the pseudorandom number generation circuits (shown in Figs. 5 & 8-9 as (101)) are "a plurality of *cascade-connected* orderly linear feedback shift registers." Cascade-connected implies that the LFSRs are not *multiple pairs* of LFSRs as required by claim 32 and also are not in "[parallel]" as stated by the Examiner. Thus, by Shimada '385 explicitly disclosing the LFSRs of element (101) as *cascade-connected* demonstrates that Shimada '385 Fig. 5 & 8-9 do not disclose or suggest *multiple pairs* of LFSRs nor could one infer *multiple pairs* of LFSRs.

Moreover, claim 32 provides that the multiple pairs of linear feedback shift registers *simultaneously produce* more than one state bit and more than one output bit for each pair..." In contrast, Shimada '385 in describing Fig. 5 in column 7, lines 45-55 explicitly states that the generator (101) "generates a pseudorandom number... and the *first* pseudorandom number is input to a *next* pseudorandom number generating circuit 101..." Applicants respectfully submit that the use of the words *first* and *next* by Shimada '385 inherently require that the plurality of linear feedback shift registers in Fig. 5 do not *simultaneously produce* more than one state bit and more than one output bit. Thus, Shimada '385 fails to disclose or suggest of multiple pairs

of LFSRs to *simultaneously produce* more than one state bit and more than one output bit for each pair of LFSRs as described in claim 32.

Turning to Shimada '099, Applicants respectfully submit that Shimada '099 in Figs. 2 & 4 merely illustrates a plurality of LFSRs, and not multiple pairs of LFSRs as provided in claim 32. Indeed, Shimada '099 when describing Fig. 2 explicitly states, "a pseudorandom number stream is outputted *serially* from the linear feedback shift registers..." in a bit-by-bit fashion. See Shimada '099, column 3, lines 18-20; and col. 7, lines 25-28. Applicants respectfully submit that use of the term *serially* in this context requires that the Shimada generator mere provides a single output, in contrast to that which is provided in claim 32.

Furthermore, when describing Fig. 4, Shimada '099 states, "each time a clock pulse of a clock pulse signal.... is inputted, a pseudorandom number is *outputted one bit by one bit* to the output terminal..." See Shimada '099, column 7, lines 25-28. Thus since Shimada '099 explicitly states a one bit by one bit output, Applicants respectfully submit that the LFSRs in Fig. 4 do not *simultaneously produce* more than one output bit.

Insofar as neither reference discloses nor could one infer from the references that multiple pairs of LFSRs simultaneously produce more than one state bit and more than one output bit for each pair, Applicants respectfully submit that the Shimada references fail to disclose or suggest all the elements of claim 32.

Thus, in summary, neither Shimada '385 nor Shimada '099 disclose or suggest each and every claim limitation of, e.g., rejected claim 32. Therefore, for at least the foregoing reasons, it is respectfully requested that the Examiner withdraw rejection of claim 32.

Applicants note that claims 33-35 depend from patentable claim 32. Thus, in addition to any independent bases for patentability, Applicants respectfully submit that claims 33-35 are

likewise patentable over the Shimada references for reasons analogous to those presented above by virtue of at least such dependency. Accordingly, Applicants respectfully request that the §103(a) rejection of claim 33-35 be withdrawn.

Claim Objections:

In paragraph 5 of the Action, claims 36-38 are objected to as being dependent upon a rejected base claim. In response, Applicants have respectfully traversed the grounds for rejection of base claim 32 as stated above. In light of this traversal, Applicants respectfully request that the objection to claims 36-38 be withdrawn.

Conclusion

For at least the foregoing reasons, Applicants respectfully submit that claims 1-6 and 12-37, as selectively amended, are in condition for allowance and such action is earnestly solicited. ***The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.***

Respectfully submitted,
Daniel J. Pugh et al.

Date: February 2, 2004 by: Paul A. Mendonsa

Paul A. Mendonsa
Reg. No. 42,879
Patent Agent for Assignee Intel Corporation

Intel Corporation
PO Box 5326
SC4-202
Santa Clara, CA 95056-5326
Tel. (503) 712.2799